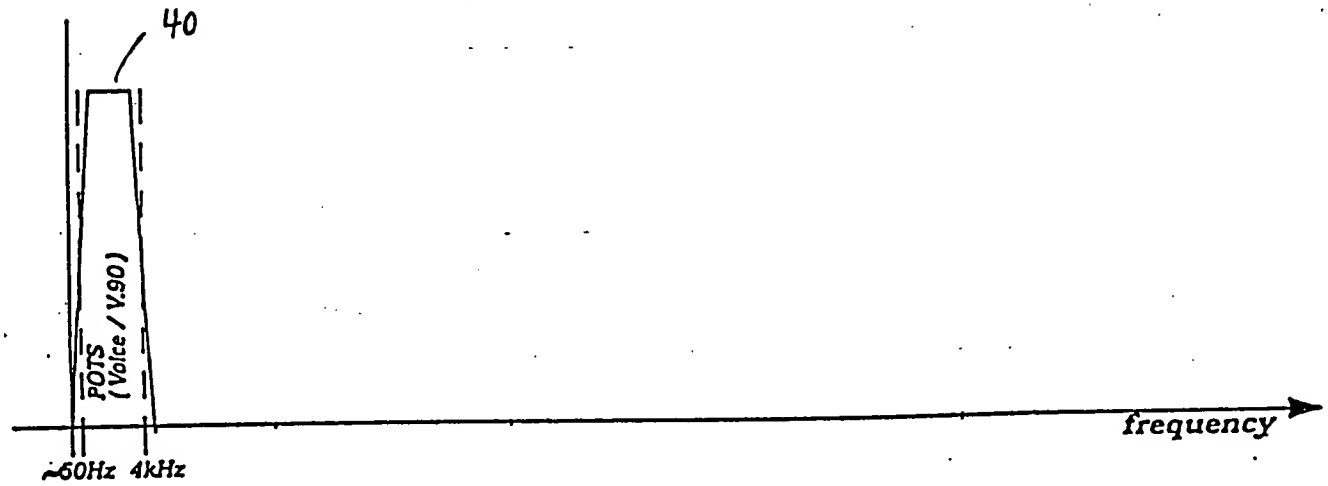

Fig 1 Prior Art

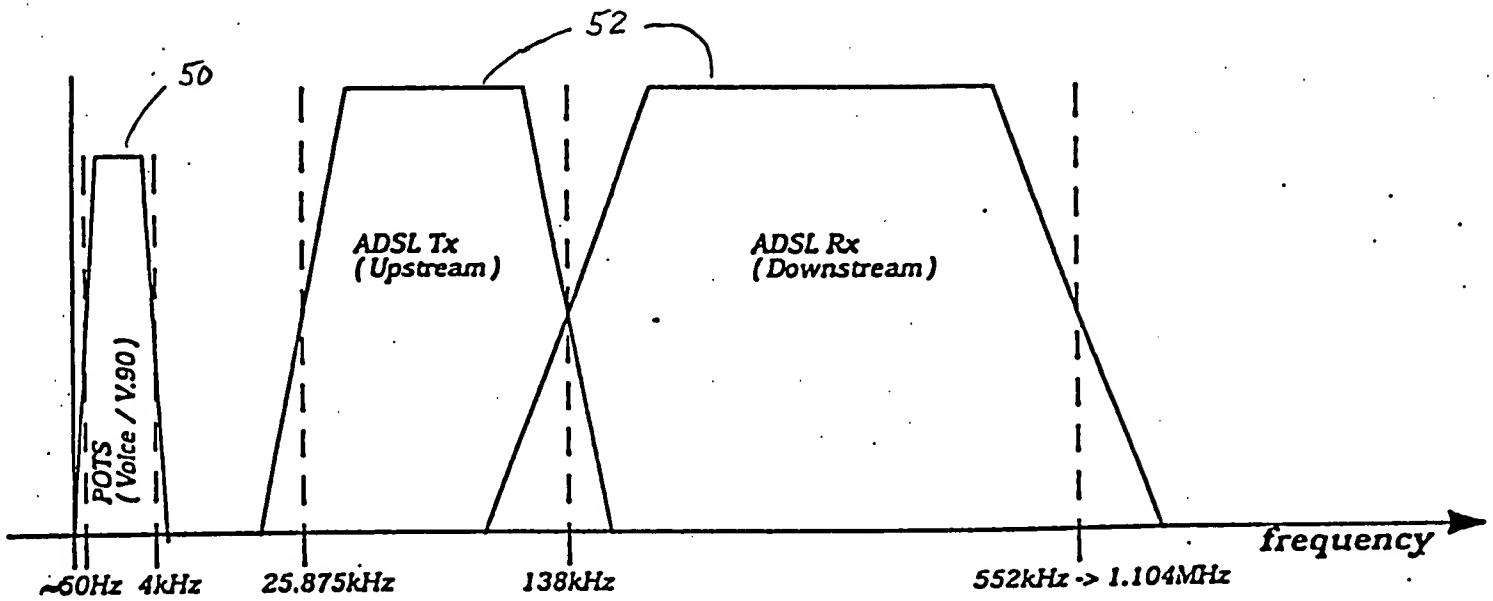

Fig 2 Prior Art

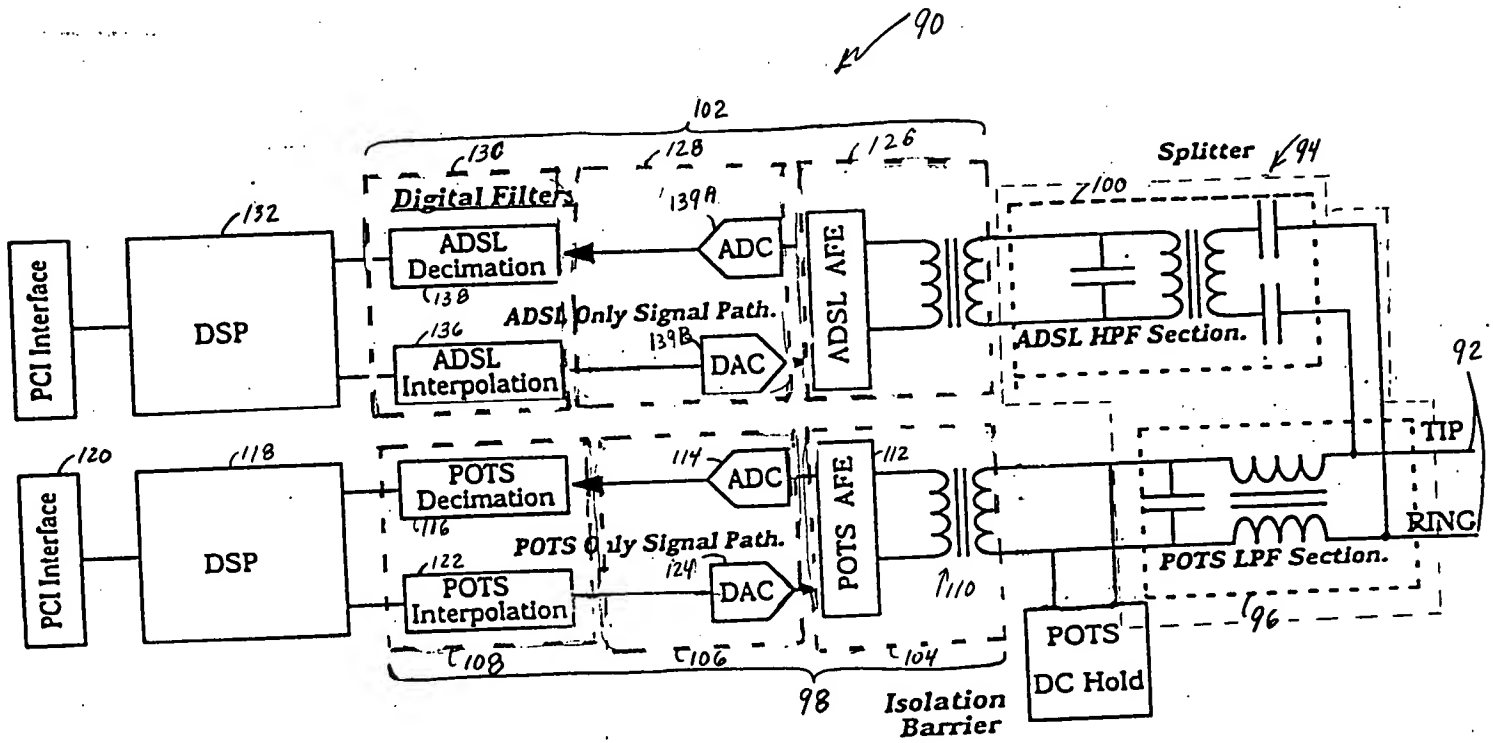

Fig. 3 Prior Art

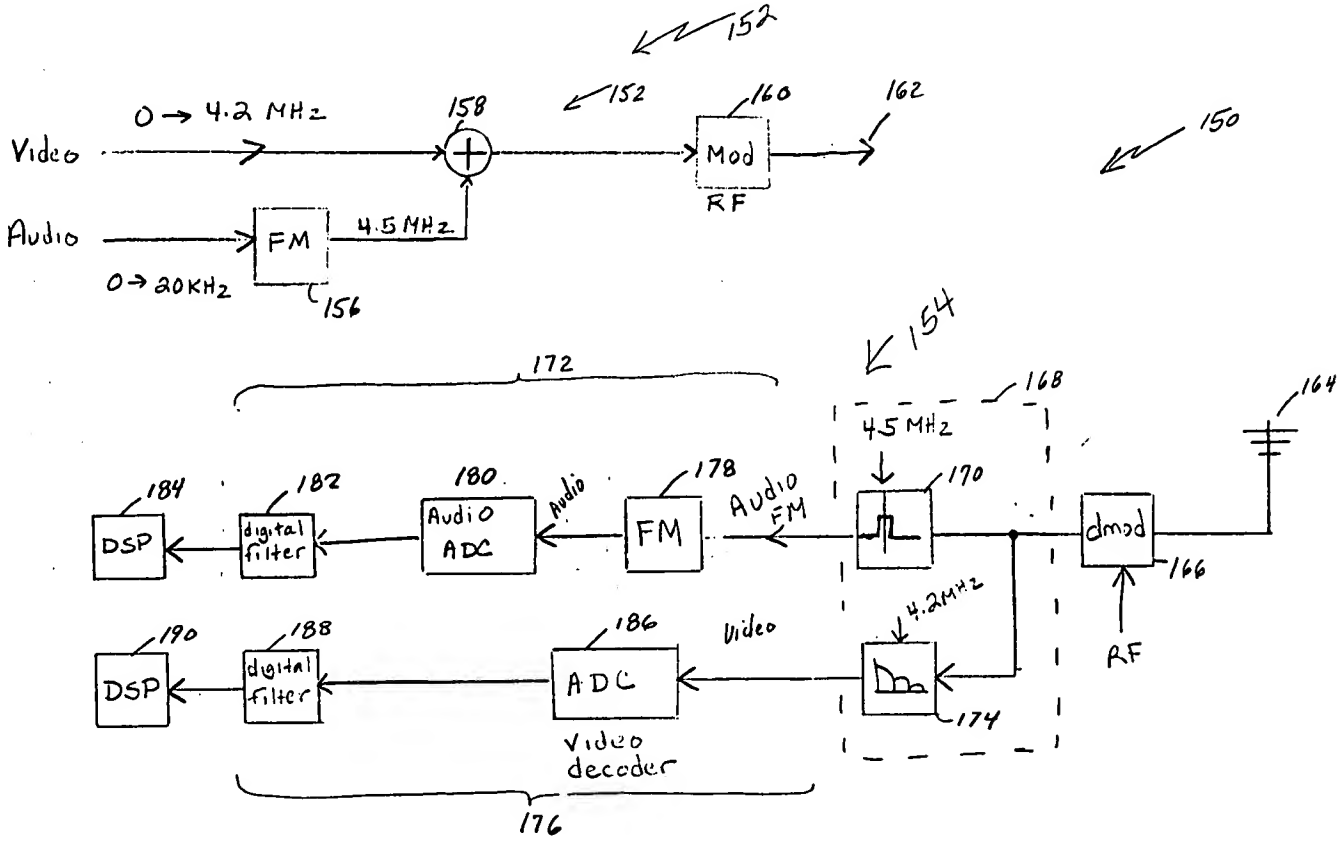

Fig 4 Prior Art

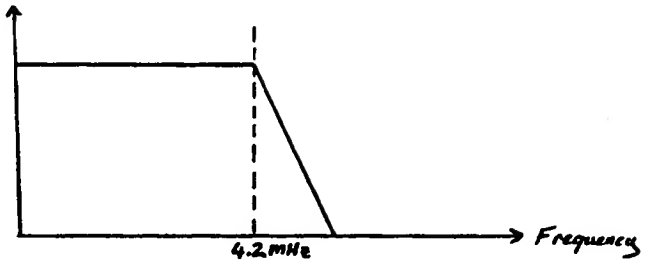

Fig. 5 Prior Art

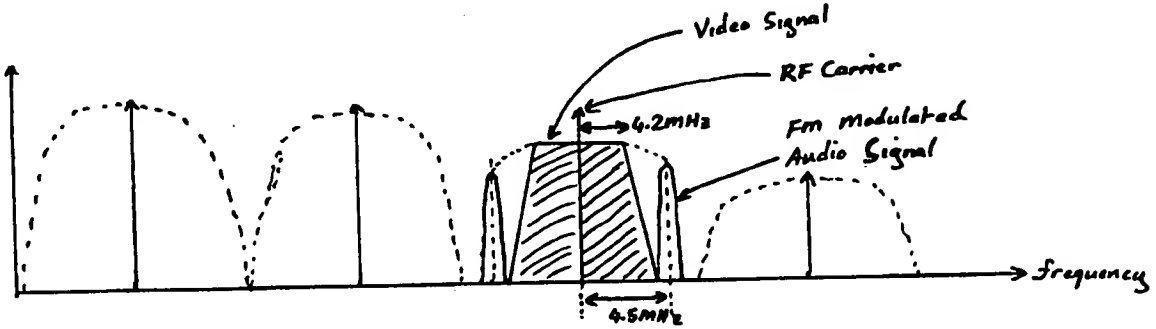

Fig 6 Prior Art

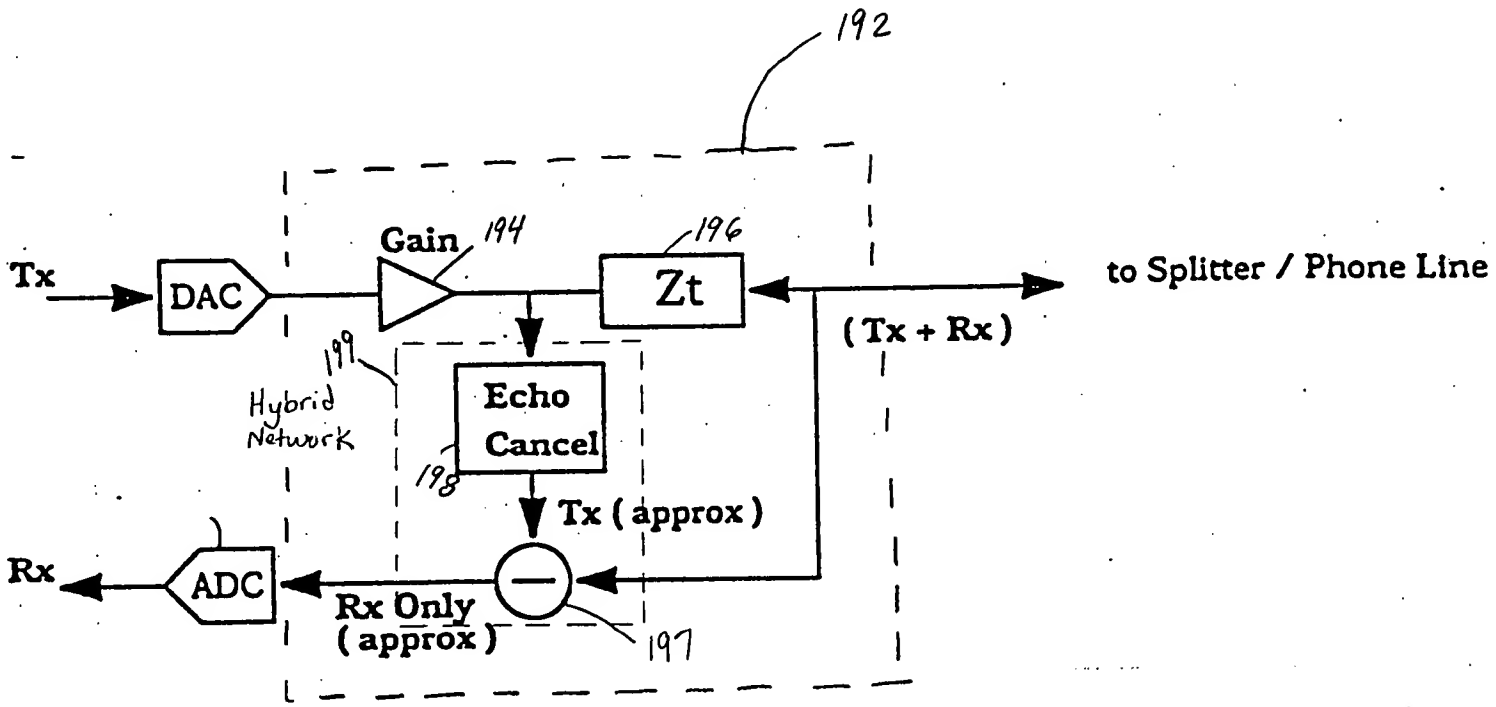

Fig. 7 Prior Art

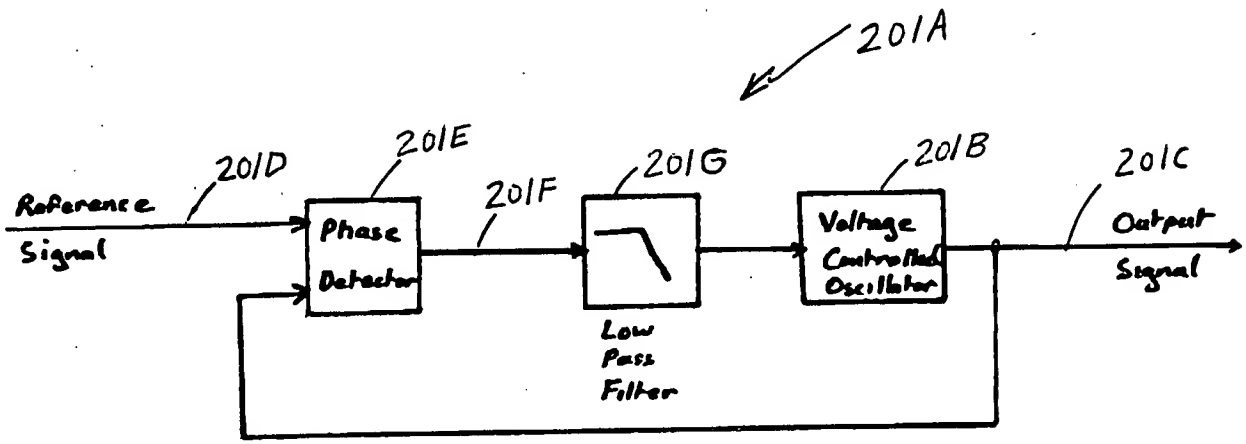

Fig 8 Prior Art

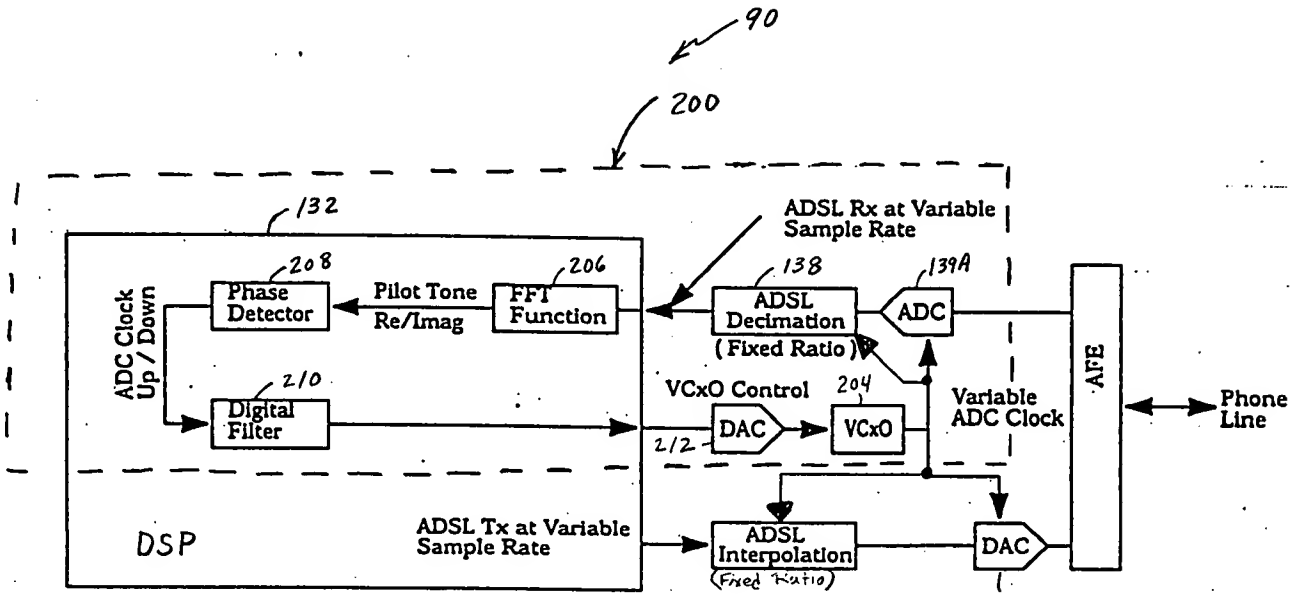

Fig. 9 Prior Art

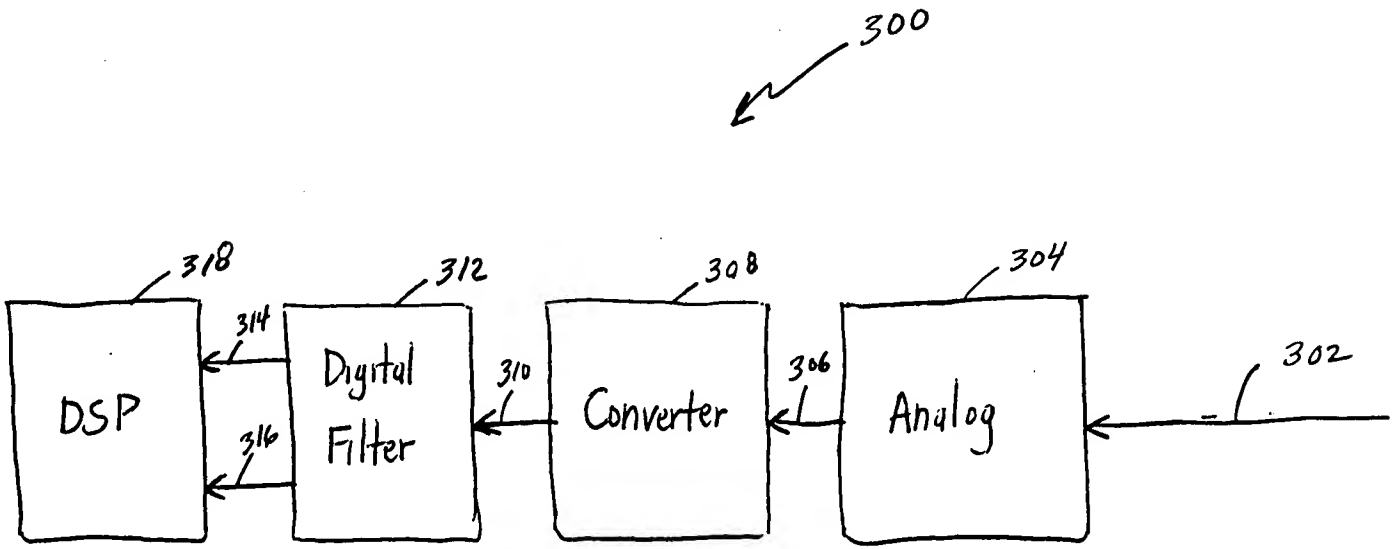
300
318
312
308
304
314
316
310
306
302
DSP
Digital Filter
Converter
Analog

Fig. 10

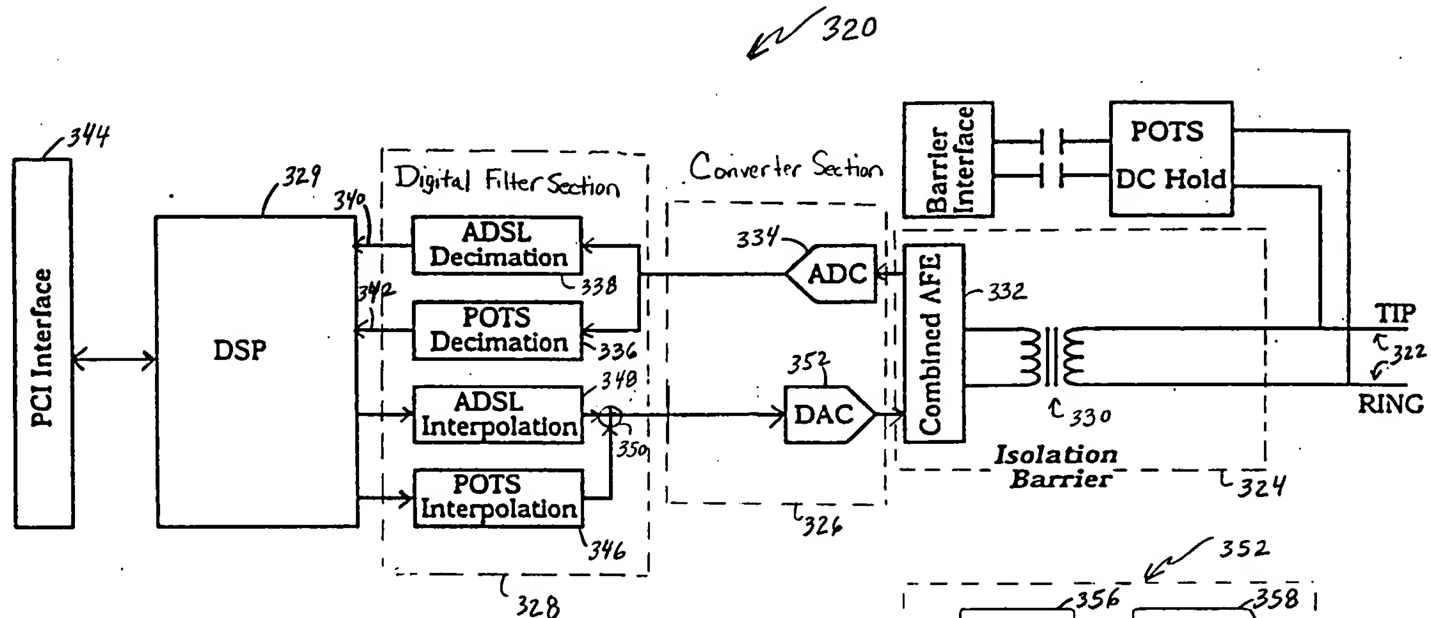

Fig. 11a

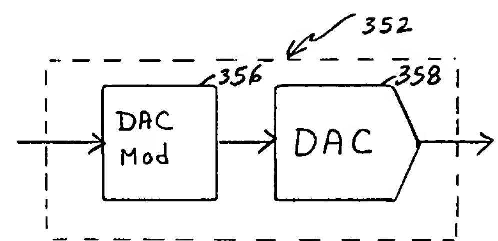

Fig. 11b

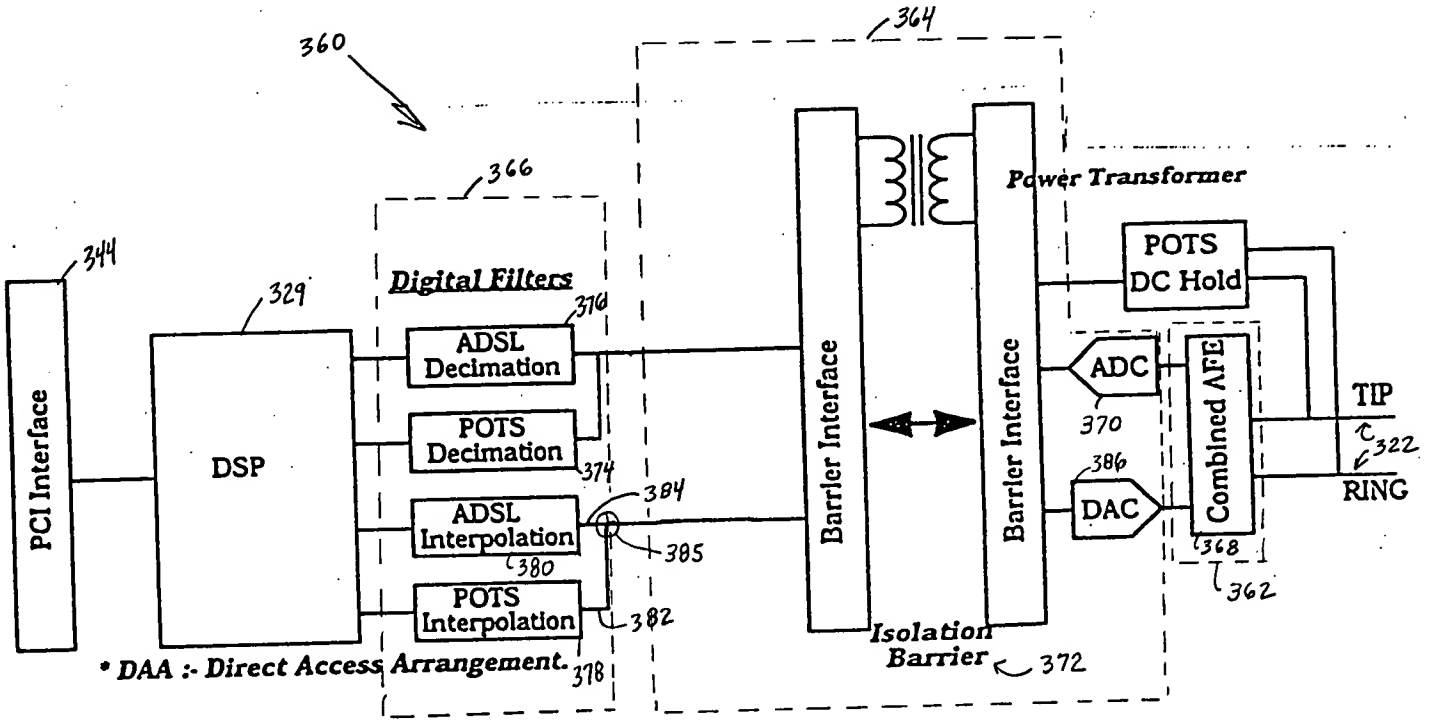

Fig. 12a

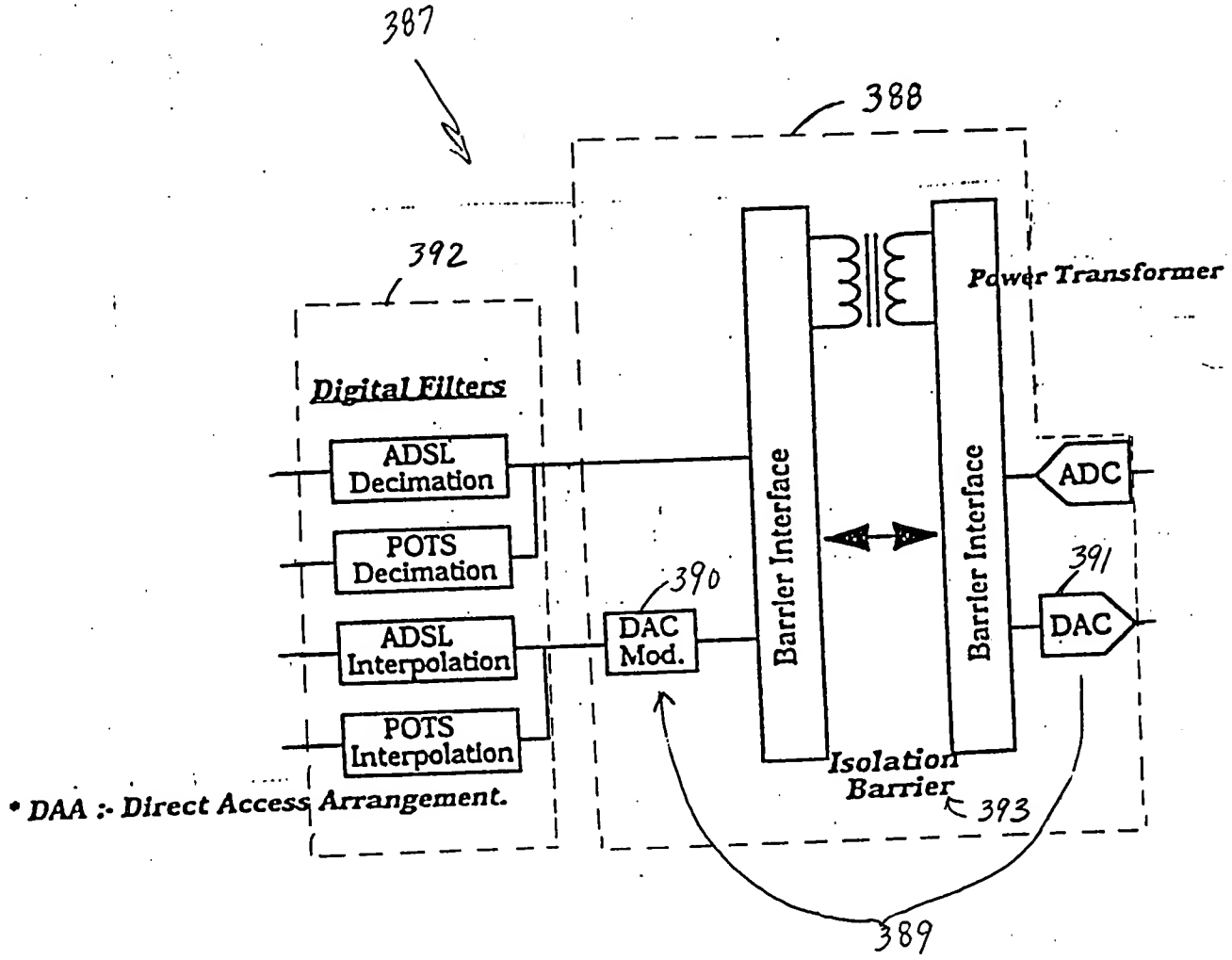

Fig. 12b

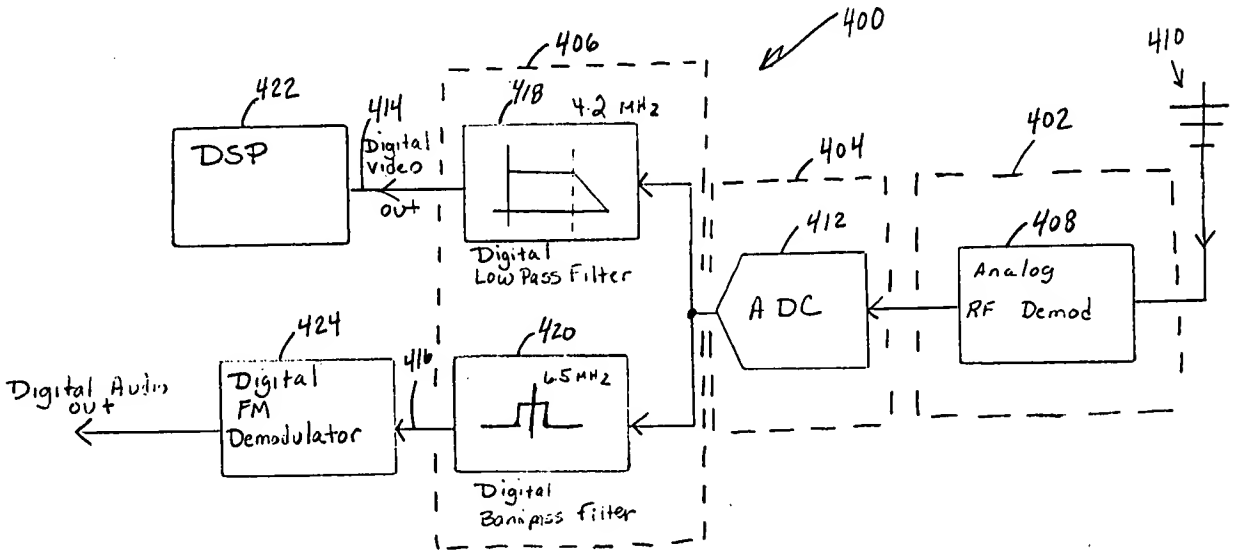
400
406
410
422
414
418
4.2 MHz
402
404
DSP
Digital Video out
Digital Low Pass Filter
412
408
Analog RF Demod
A DC
424
420
416
6.5 MHz
Digital Audio out
Digital FM Demodulator
Digital Bandpass Filter

Fig. 13

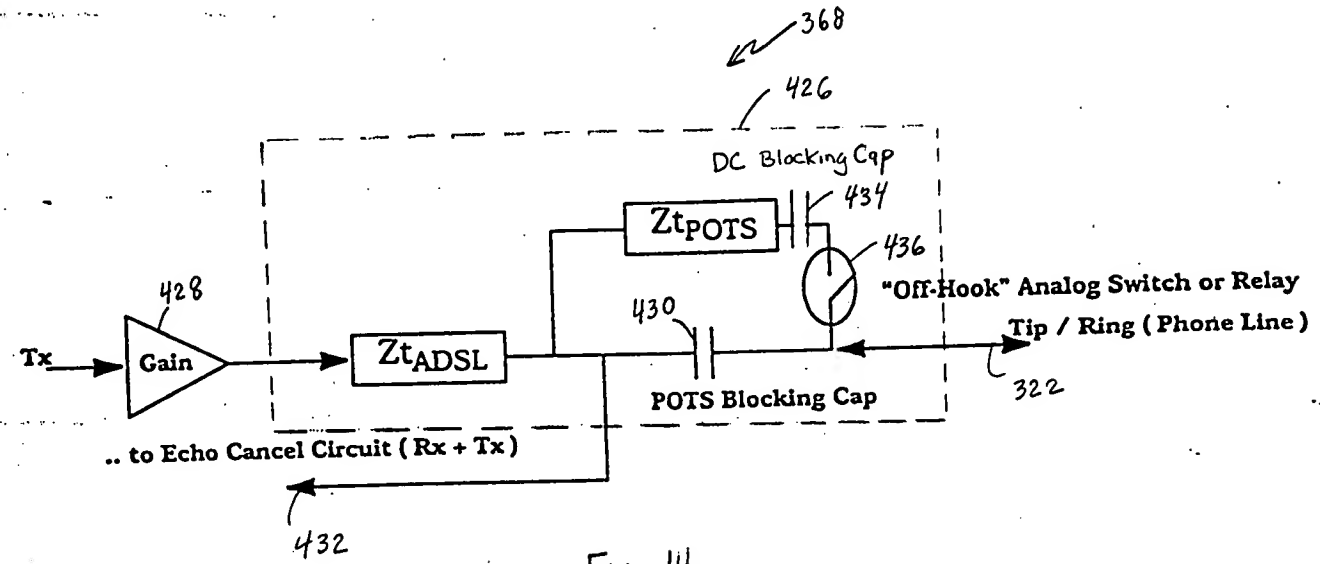

Fig. 14a

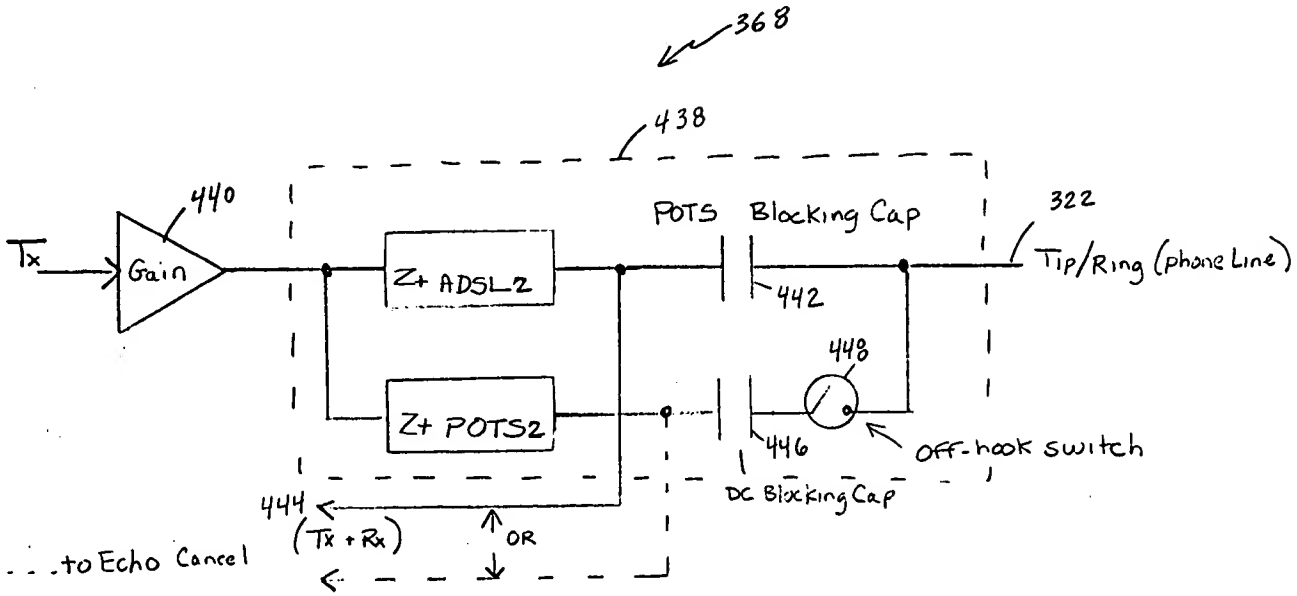

Fig 14b

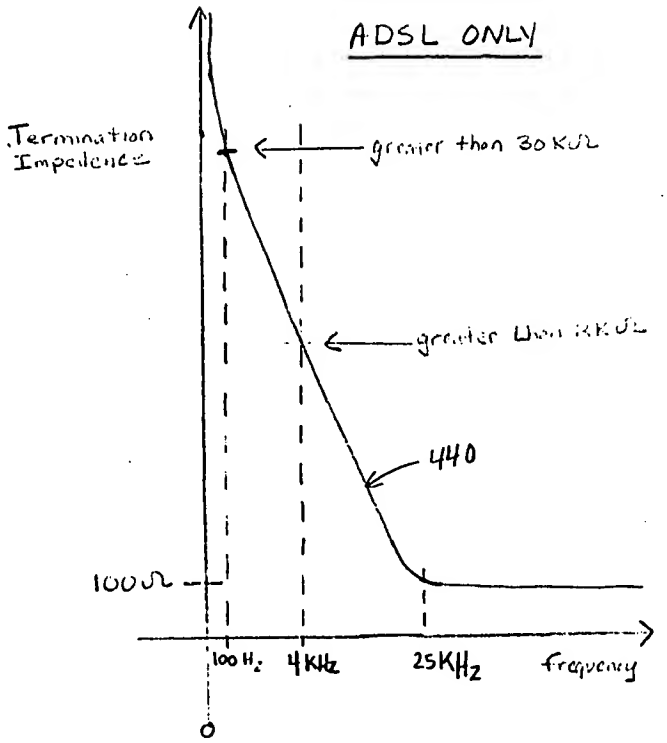

Fig. 15a

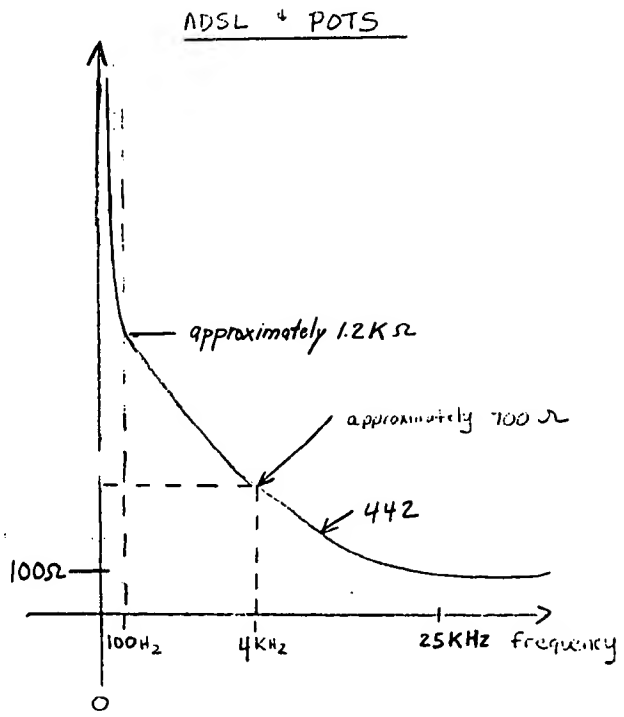

Fig. 15b

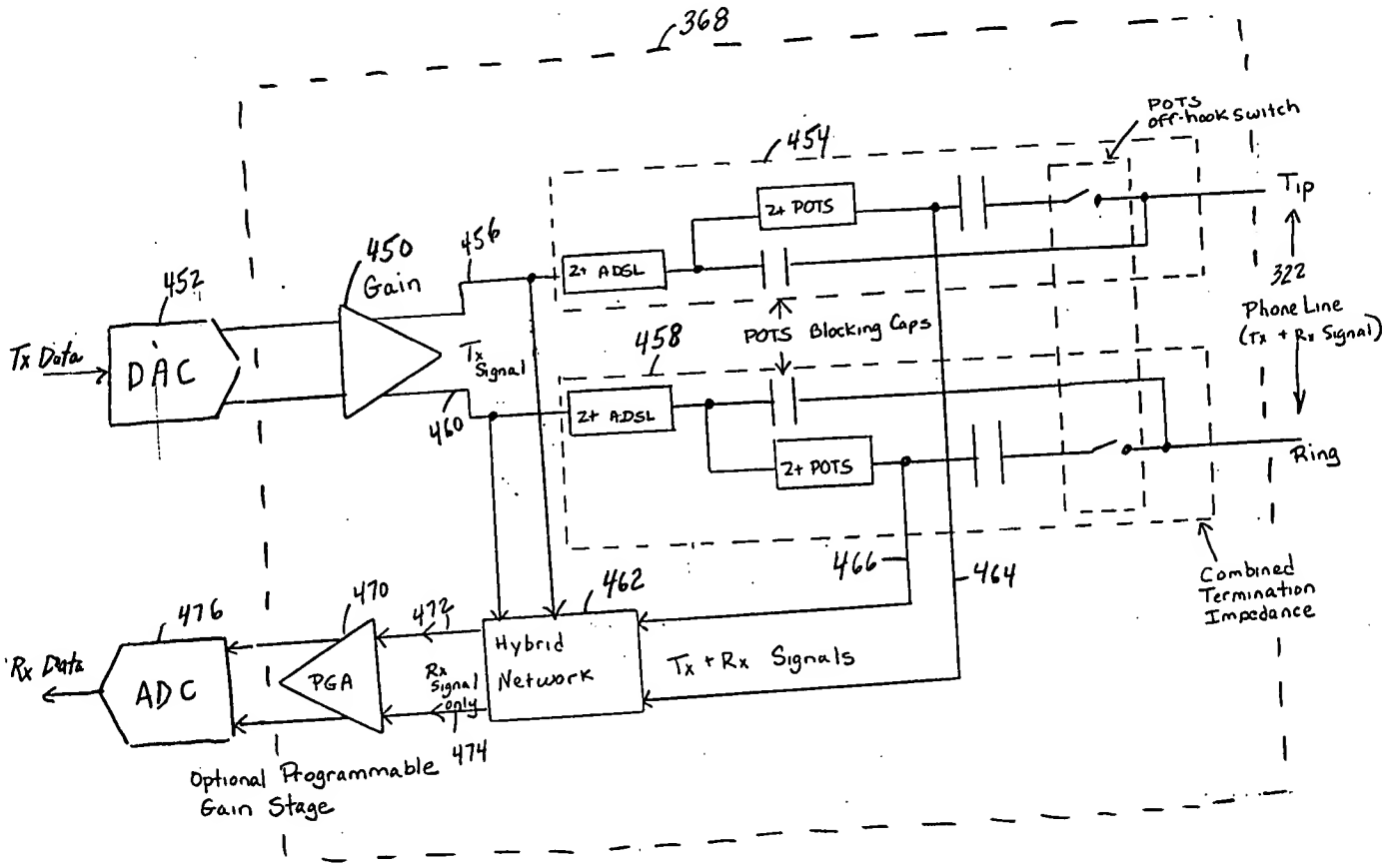
368
454
POTS off-hook switch
Tip
322
Phone Line (Tx + Rx Signal)
Ring
Combined Termination Impedance
452
450 Gain
456
Tx Data
DAC
Tx Signal
460
2+ POTS
2+ ADSL
POTS Blocking Caps
458
2+ ADSL
2+ POTS
466
464
462
470
472
476
Rx Data
ADC
PGA
Rx Signal only
Hybrid Network
Tx + Rx Signals
474
Optional Programmable Gain Stage

Fig 16a

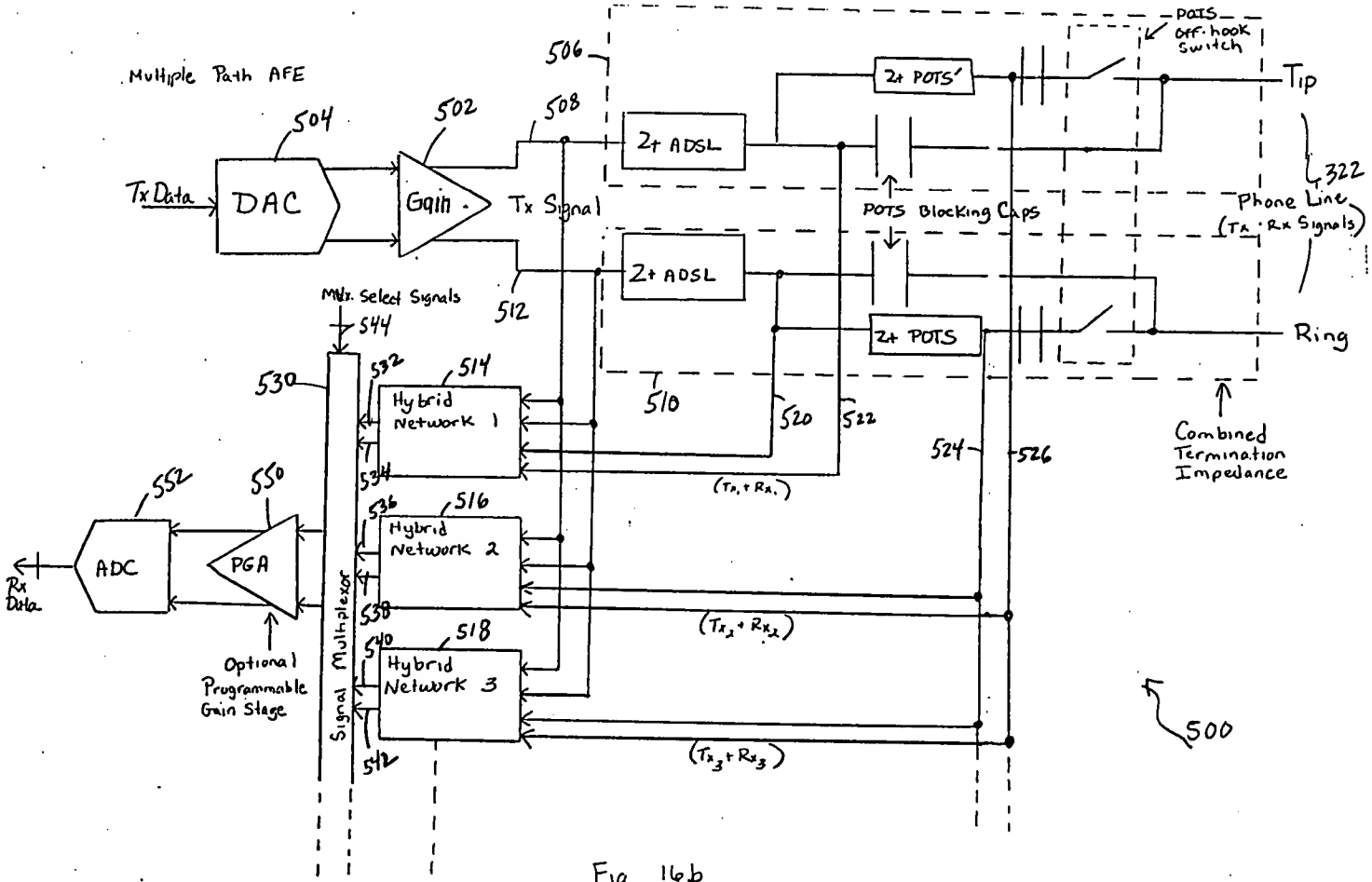
Multiple Path AFE
504
502
506
508
Tx Data
DAC
Gain
Tx Signal
2+ ADSL
2+ POTS
POTS off-hook Switch
Tip
322
Phone Line (Tx + Rx Signals)
POTS Blocking Caps
2+ ADSL
2+ POTS
Ring
Mux. Select Signals
544
512
530
532
514
Hybrid Network 1
510
520
522
524
526
Combined Termination Impedance
534
(Tx1 + Rx1)
552
550
516
Hybrid Network 2
ADC
PGA
Rx Data
536
538
(Tx2 + Rx2)
Optional Programmable Gain Stage
Signal Multiplexor
540
518
Hybrid Network 3
542
(Tx3 + Rx3)
500

Fig 16b

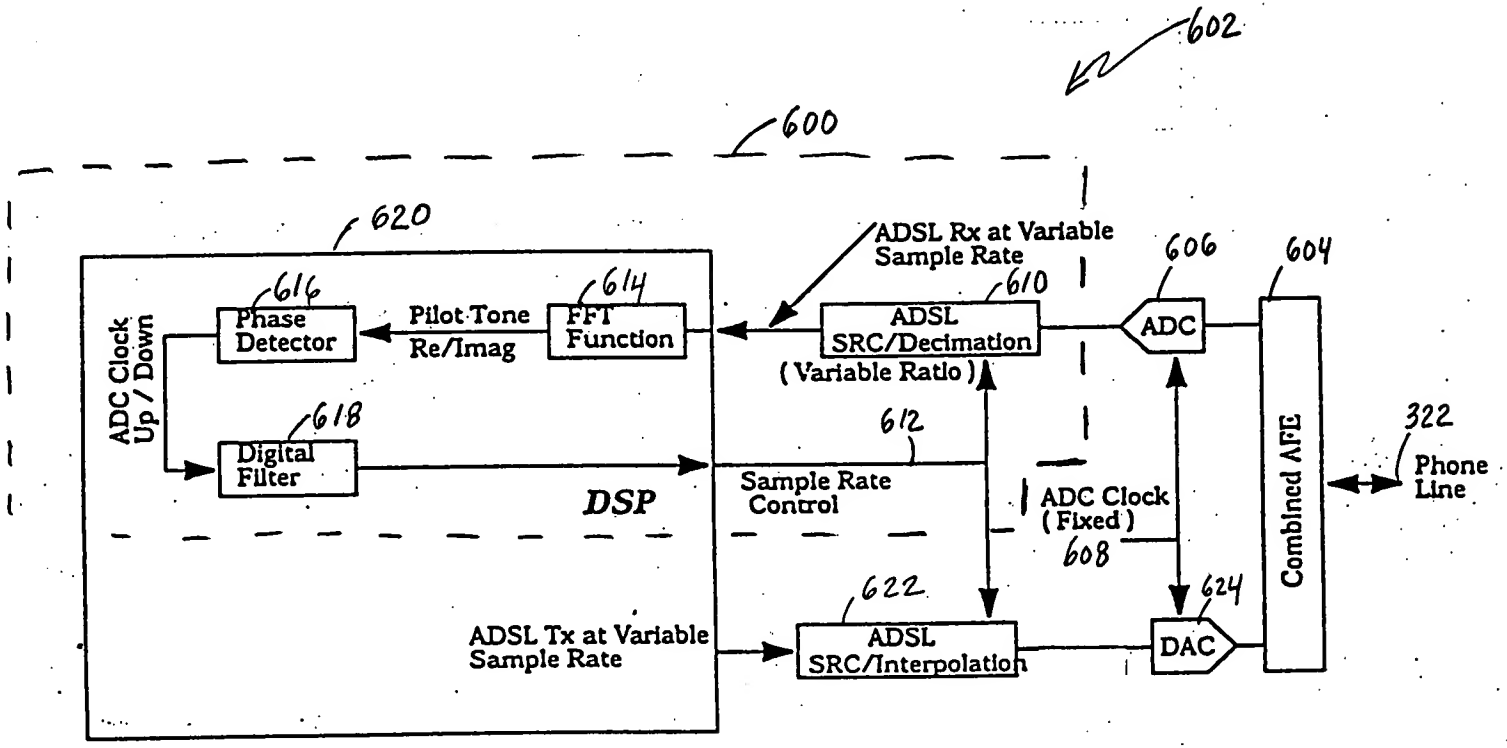

Fig. 17

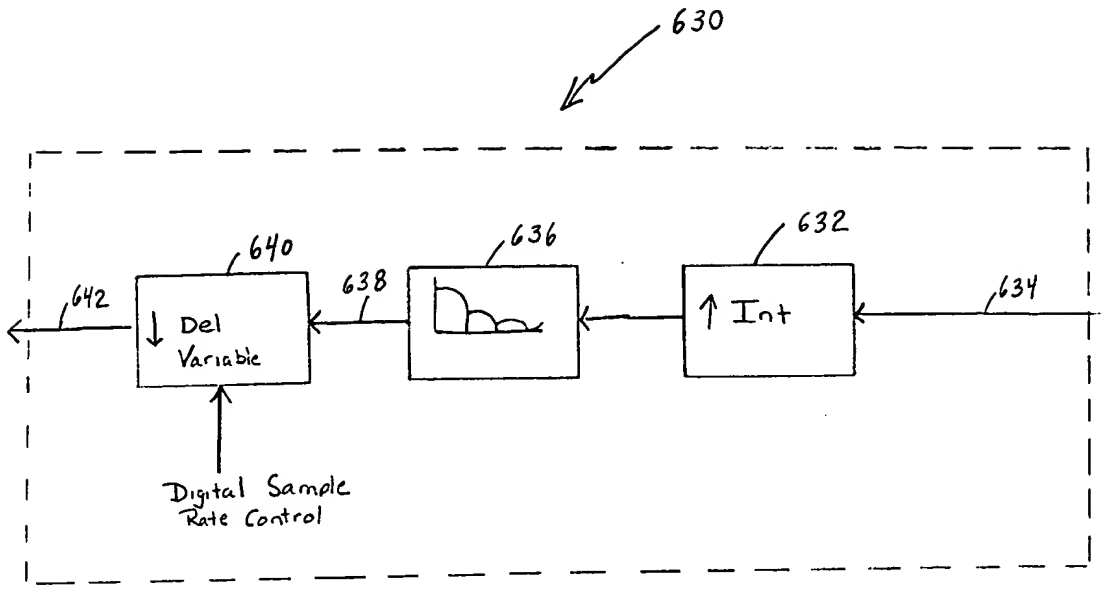
630
640
636
632
642
638
634
↓ Del
Variable
↑ Int
Digital Sample
Rate Control

Fig 18

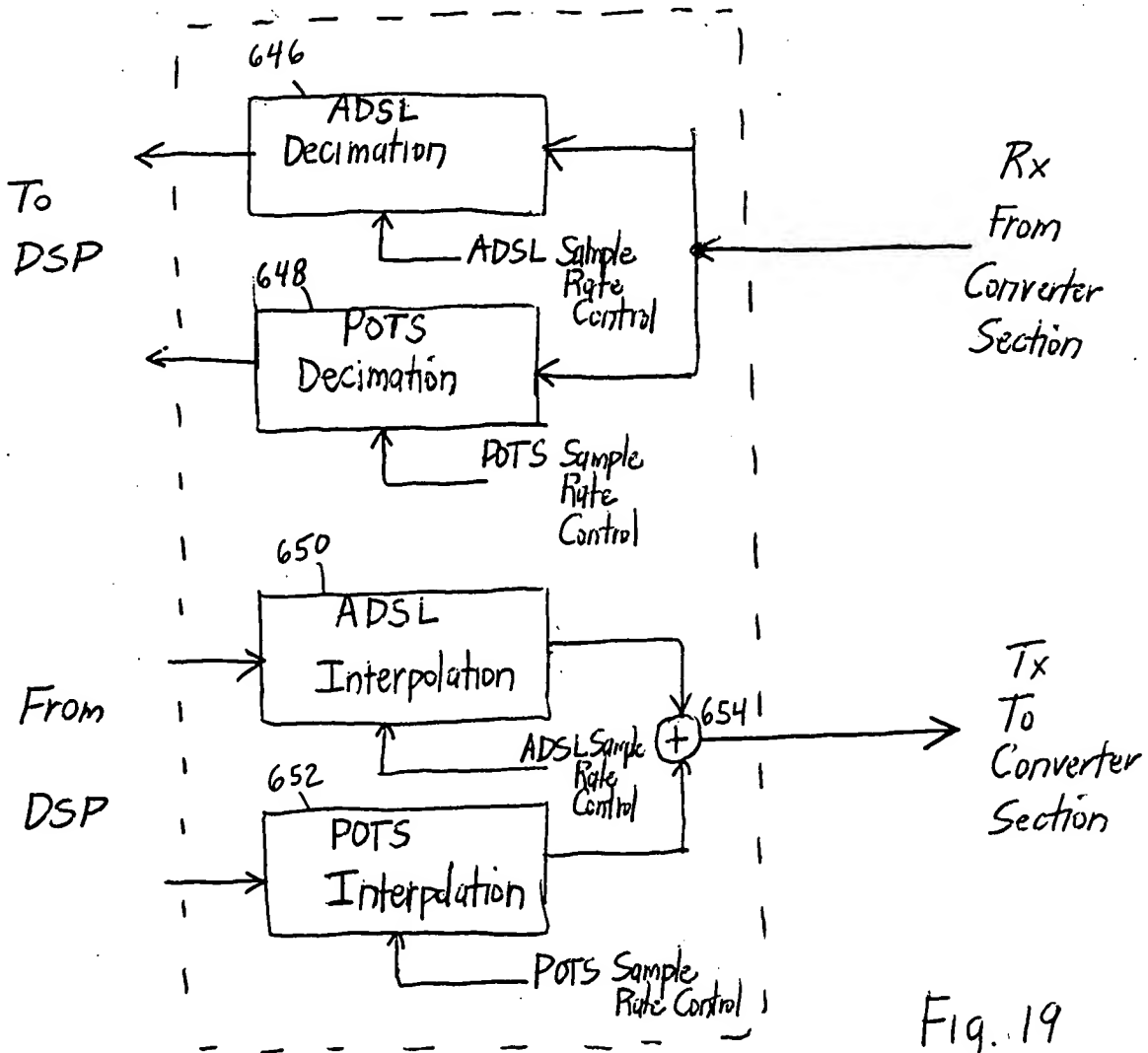
646
ADSL Decimation
To DSP
ADSL Sample Rate Control
Rx From Converter Section
648
POTS Decimation
POTS Sample Rate Control
650
ADSL Interpolation
From DSP
654
ADSL Sample Rate Control
Tx To Converter Section
652
POTS Interpolation
POTS Sample Rate Control

Fig. 19

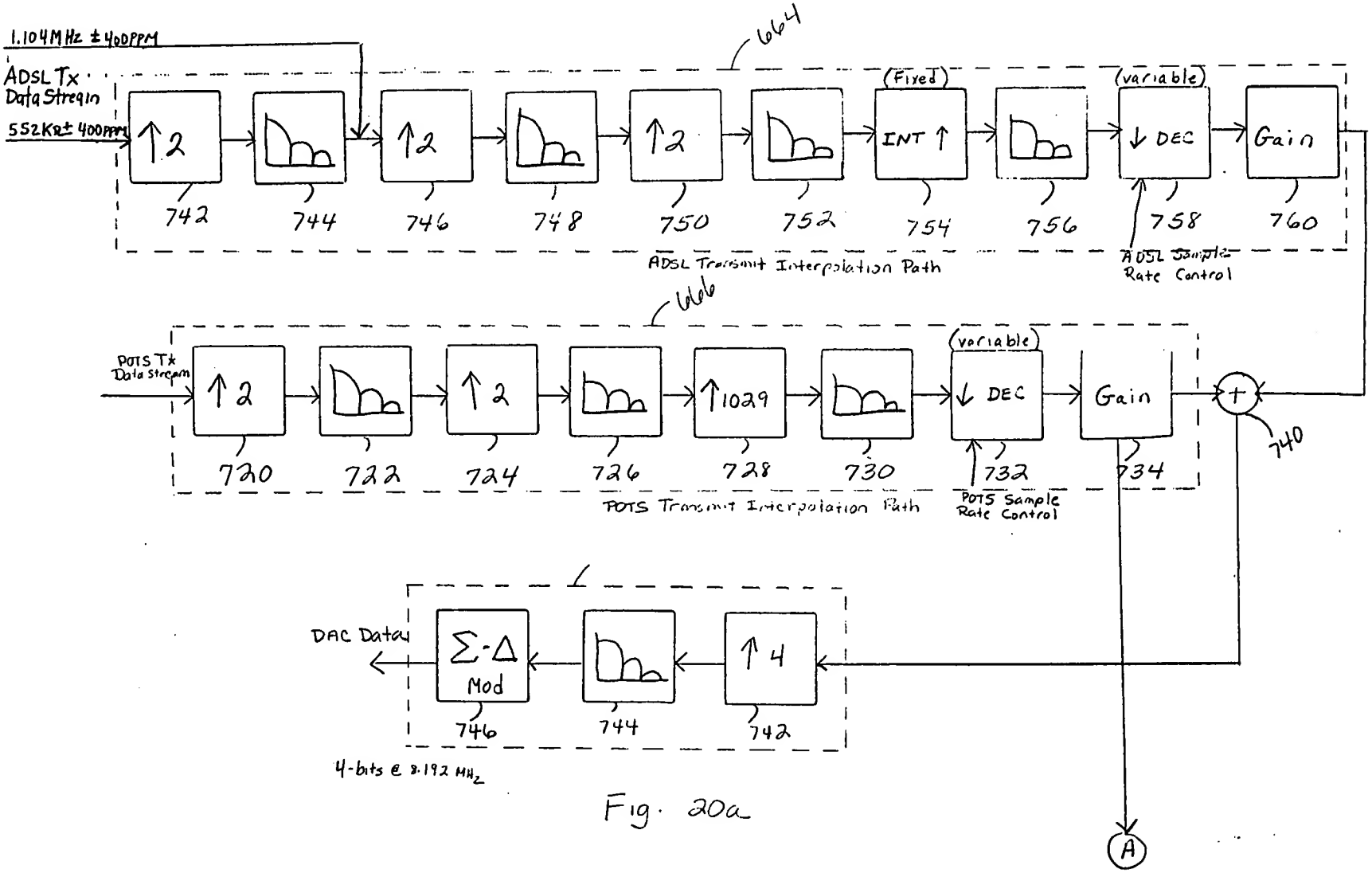
1.104MHz ±400PPM
ADSL Tx Data Stream
552Kz± 400PPM
664
↑2
↑2
↑2
INT ↑
(Fixed)
↓ DEC
(variable)
Gain
742
744
746
748
750
752
754
756
758
760
ADSL Transmit Interpolation Path
ADSL Sample Rate Control
666
POTS Tx Data Stream
↑2
↑2
↑1029
↓ DEC
(variable)
Gain
720
722
724
726
728
730
732
734
740
POTS Transmit Interpolation Path
POTS Sample Rate Control
DAC Data
Σ-Δ Mod
↑4
746
744
742
4-bits @ 8.192 MHz
A

Fig. 20a

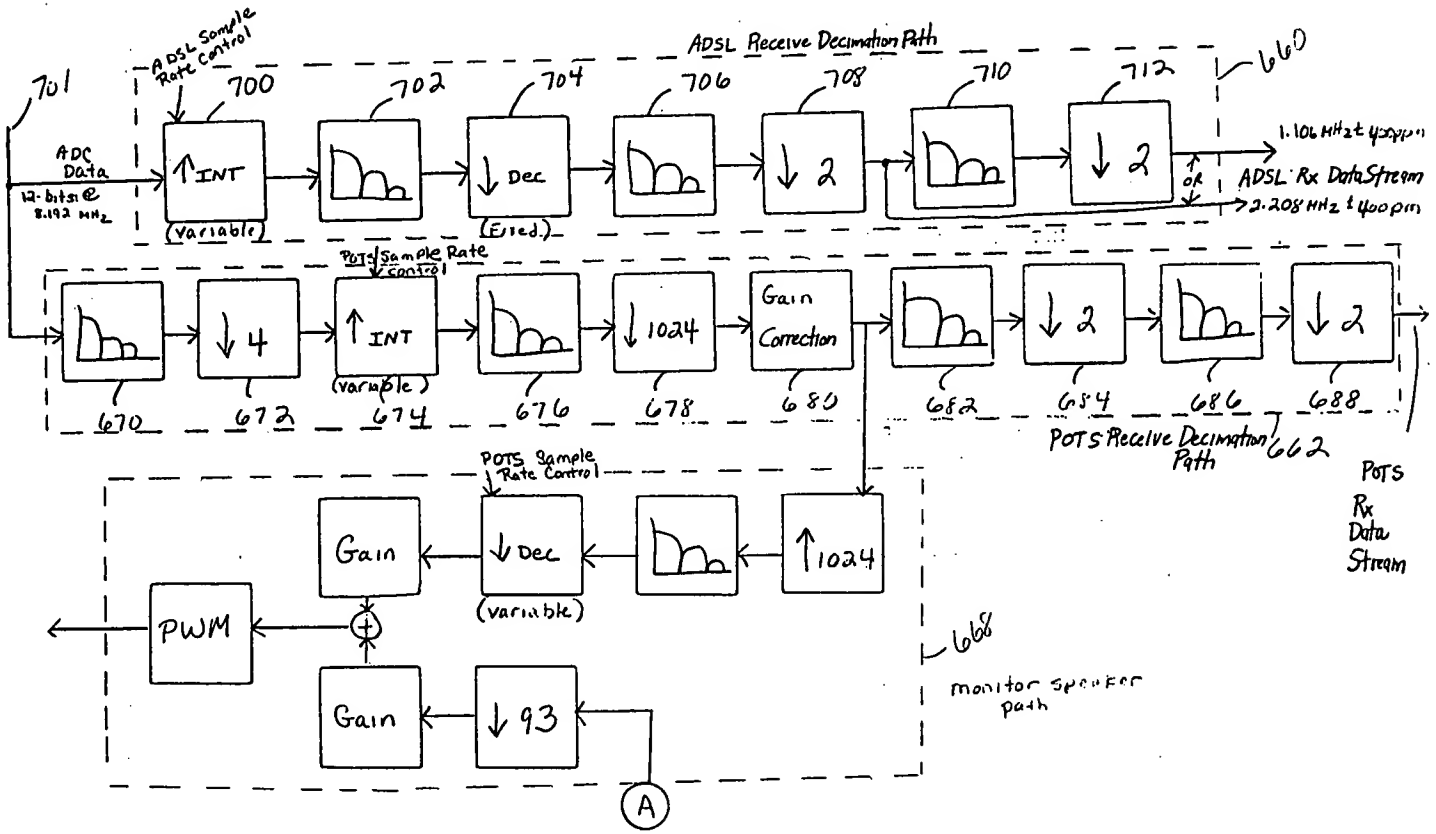

Fig 20b

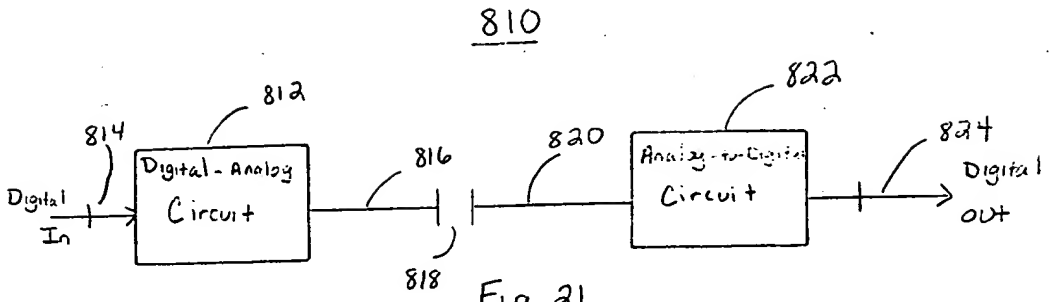

Fig. 21

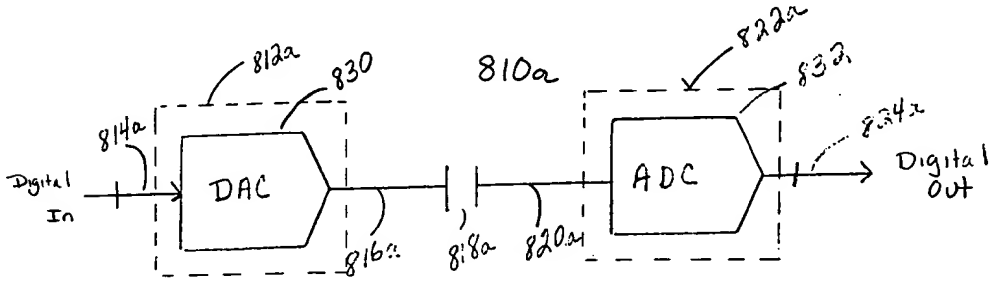

Fig. 22

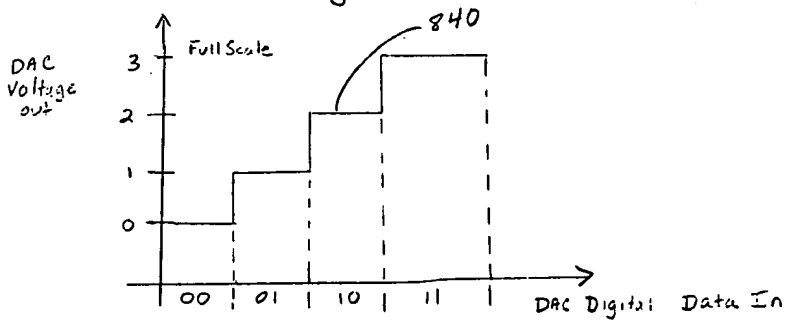

Fig. 23

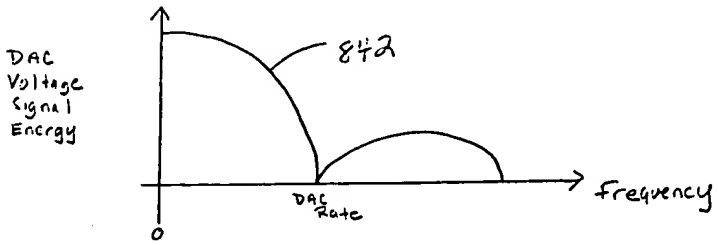

Fig. 24

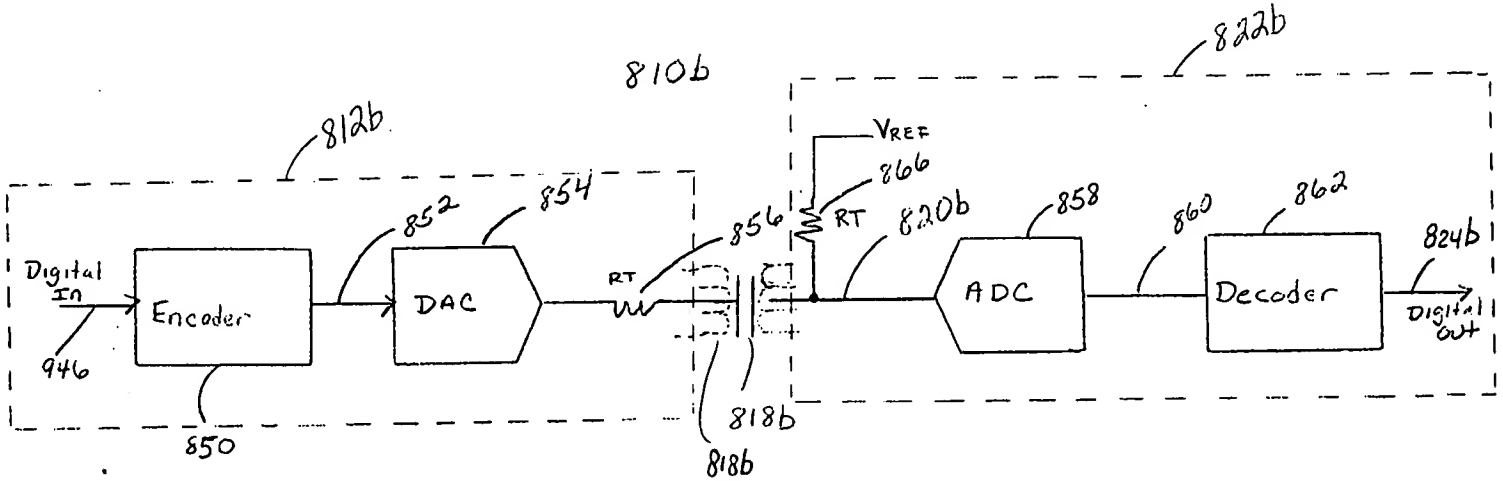
810b
822b
812b
VREF
866
RT
820b
858
860
862
824b
852
854
856
Digital In
Encoder
DAC
RT
ADC
Decoder
Digital Out
946
850
818b
818b

Fig 25

ENCODER

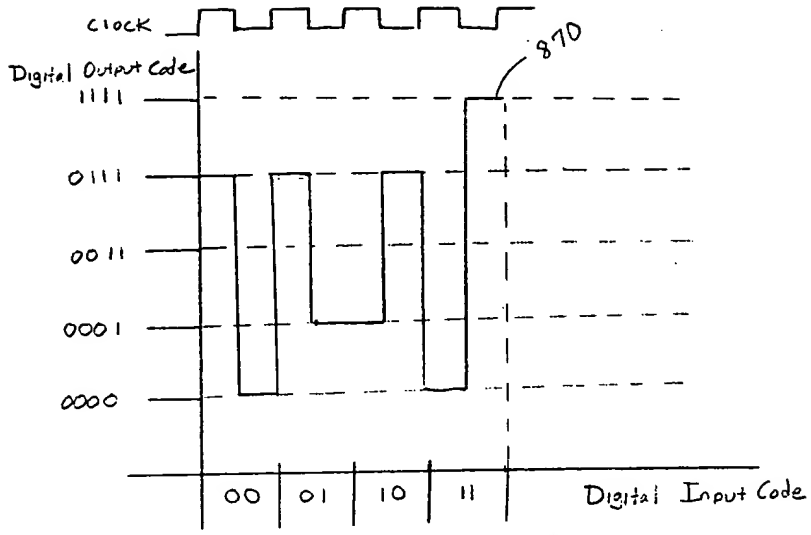

Fig 26

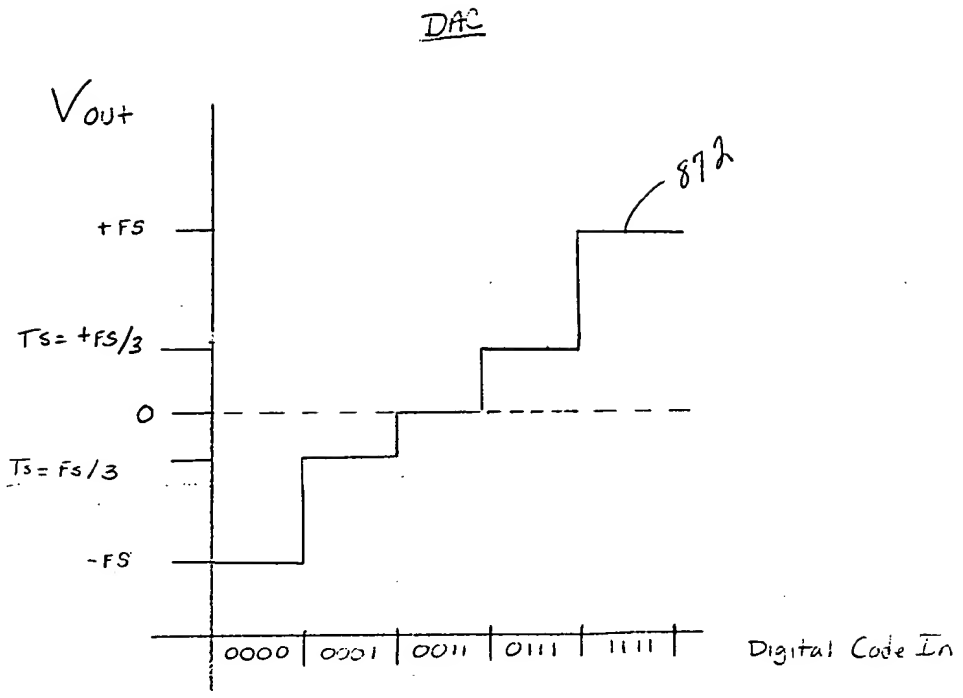
DAC
V_{OUT}
+FS
Ts = +FS/3
0
Ts = Fs/3
-FS
872
0000
0001
0011
0111
1111
Digital Code In

Fig. 27

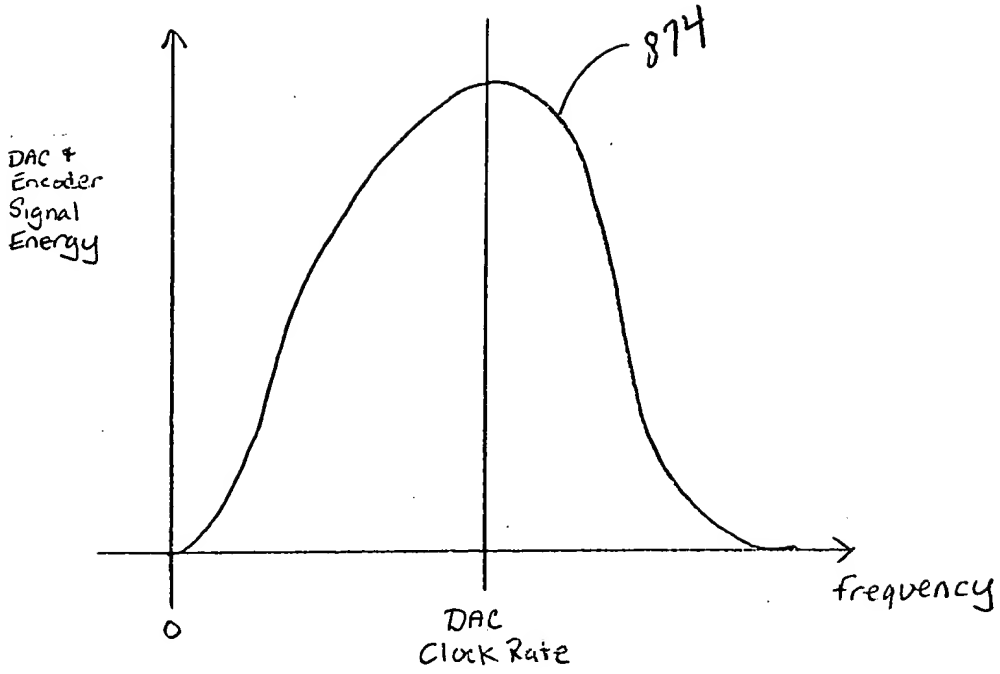

Fig. 28

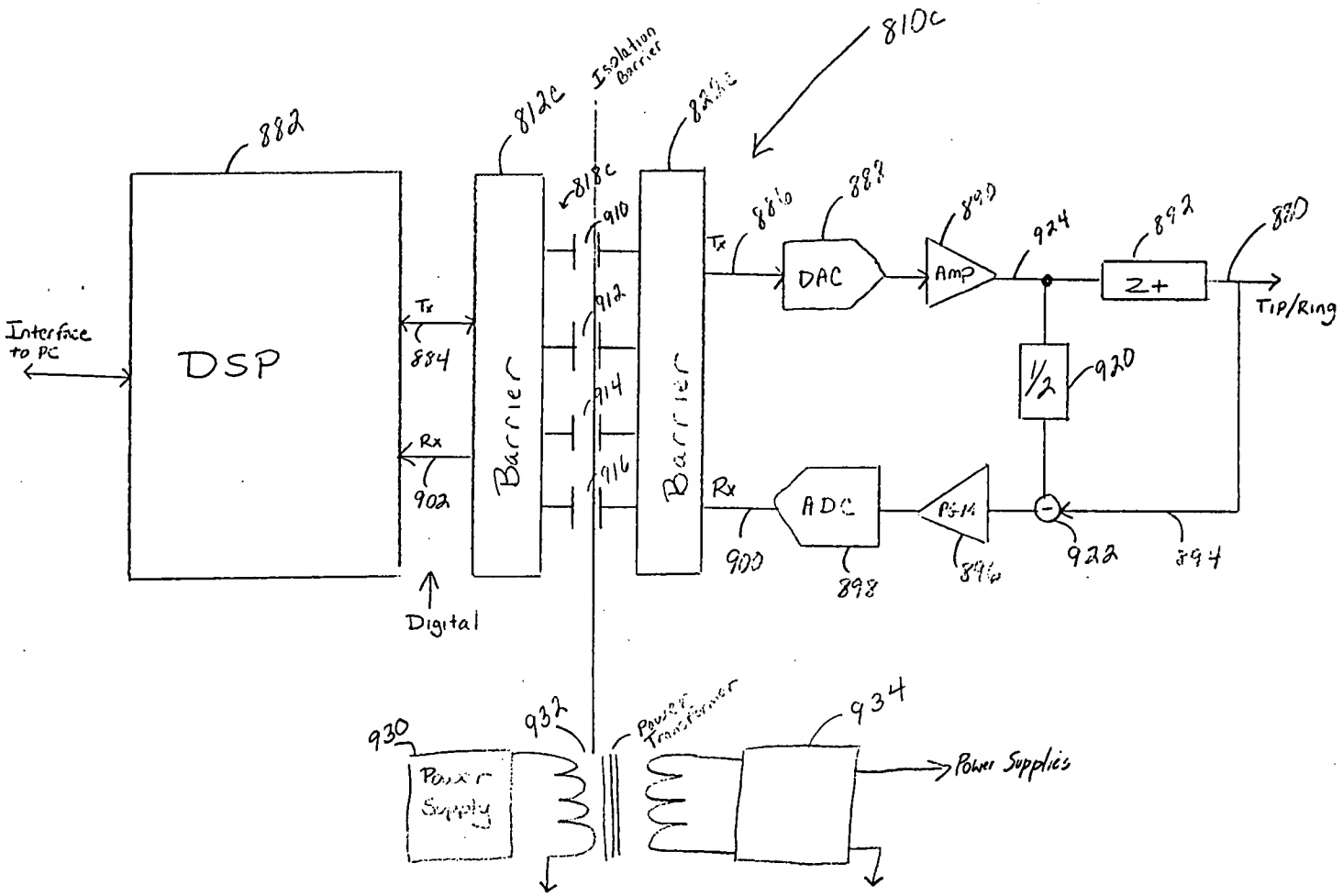
810c
882
812c
Isolation Barrier
818c
910
912
914
916
Interface to PC
DSP
Tx
884
Rx
902
Barrier
Barrier
Tx
Rx
DAC
Amp
924
2+
880
Tip/Ring
1/2
920
ADC
922
894
900
898
Digital
930
932
Power Transformer
934
Power Supply
Power Supplies

Fig. 29

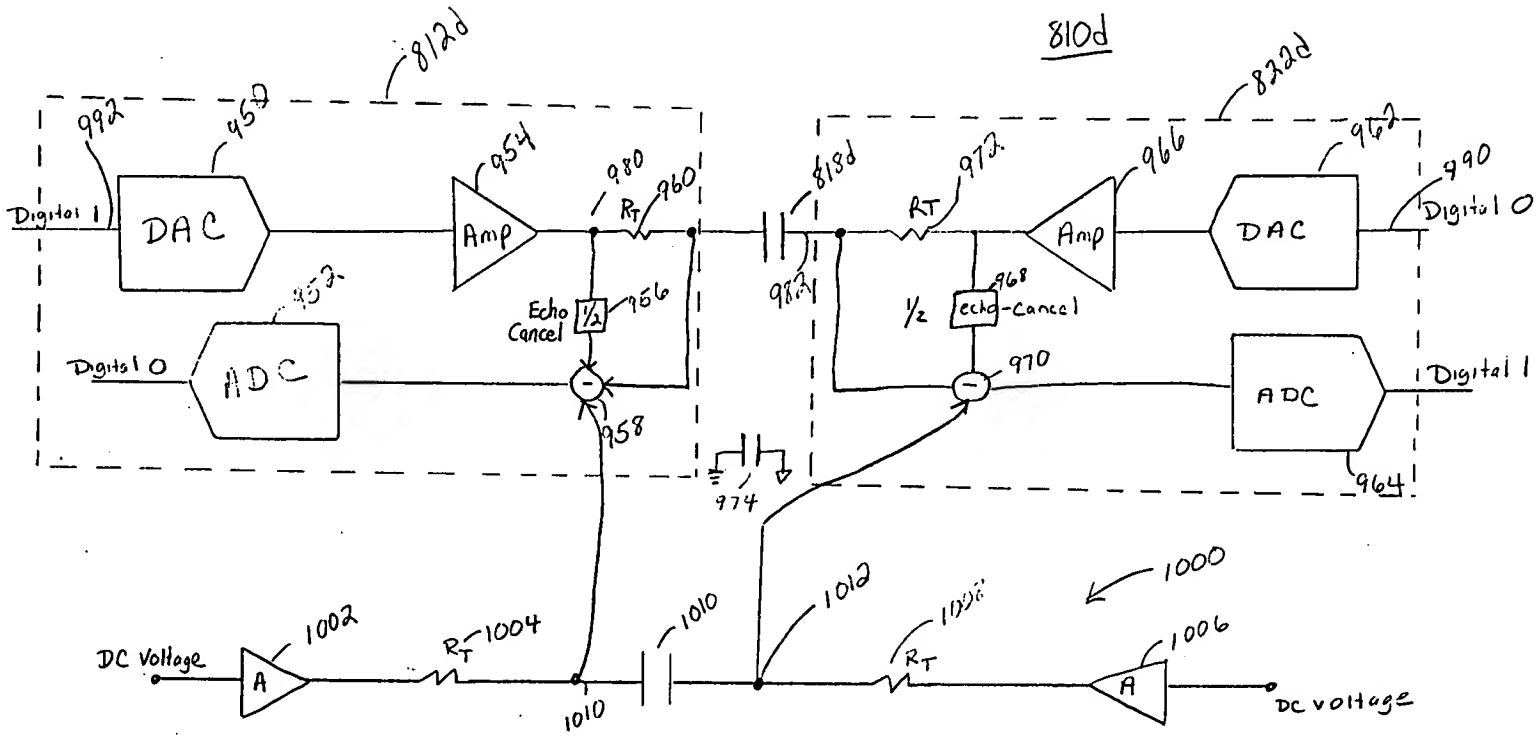
812d
810d
832d
992
952
954
980
960
818d
972
966
962
990
Digital I
DAC
Amp
RT
Amp
DAC
Digital O
Echo Cancel
1/2
956
968
1/2
echo-cancel
ADC
Digital O
ADC
Digital I
970
958
964
974
1000
DC Voltage
A
1002
RT
1004
1010
1012
RT
1006
A
DC voltage

Fig 30

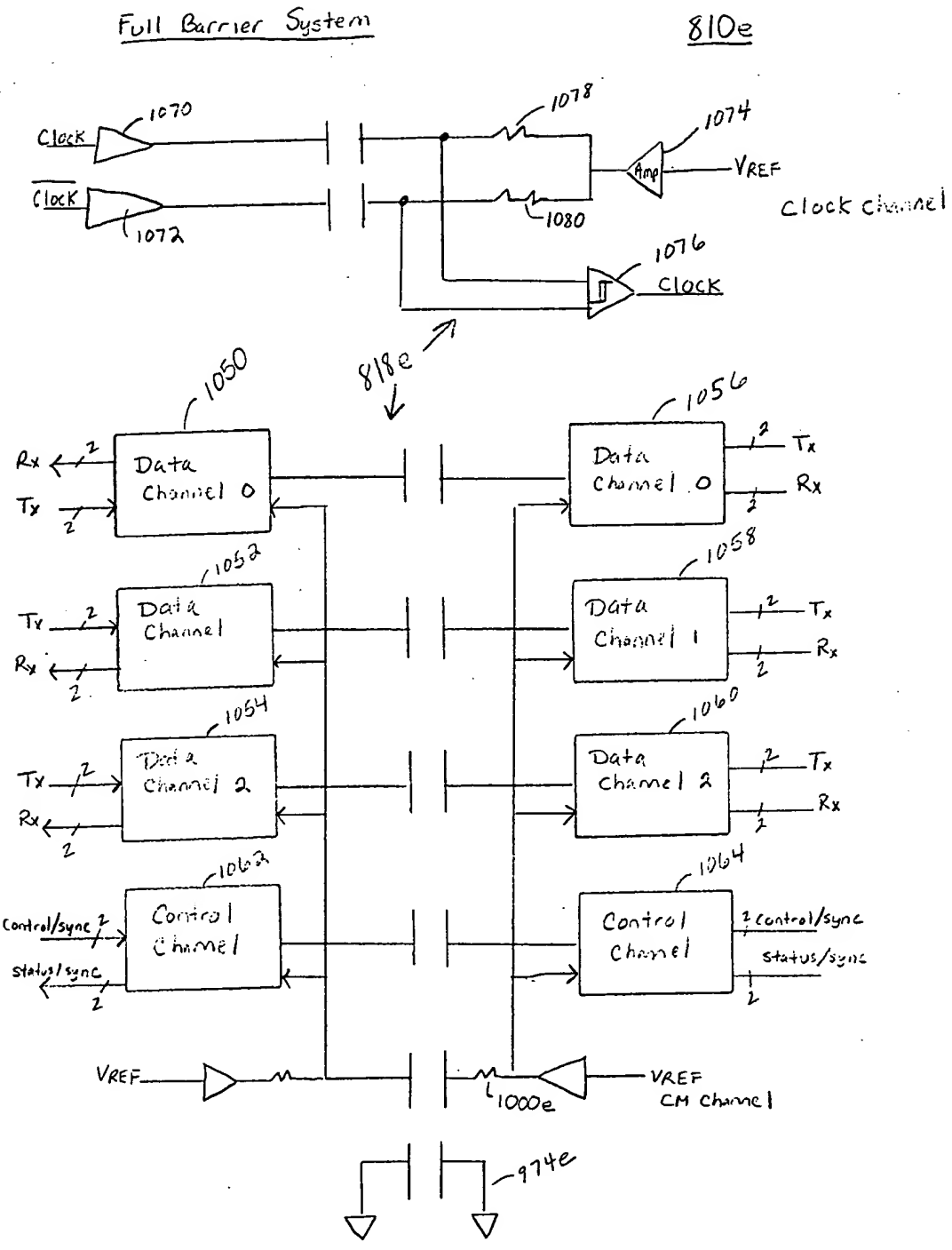
Full Barrier System
810e
Clock
1070
Clock
1072
1078
1080
1074
Amp
VREF
Clock channel
1076
Clock
818e
1050
Data Channel 0
Rx
Tx
1052
Data Channel
Tx
Rx
1054
Data Channel 2
Tx
Rx
1062
Control Channel
Control/sync
status/sync
1056
Data Channel 0
Tx
Rx
1058
Data Channel 1
Tx
Rx
1060
Data Channel 2
Tx
Rx
1064
Control Channel
Control/sync
status/sync
VREF
1000e
VREF
CM Channel
974e

Fig. 31

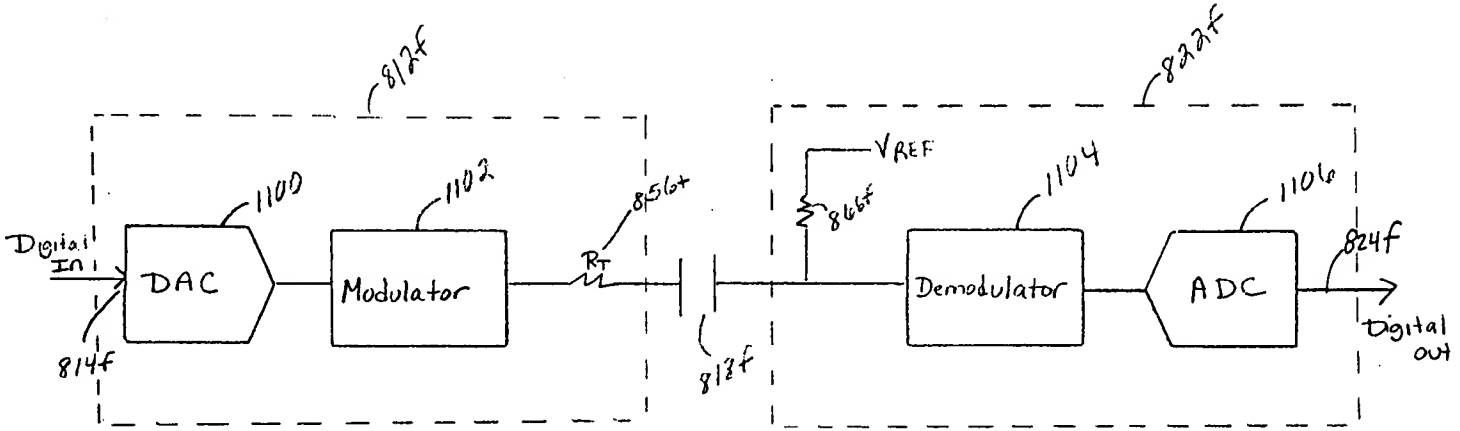

Fig. 32